Dual VCO/PLL Synthesizer With IF Upconverter

FEATURES

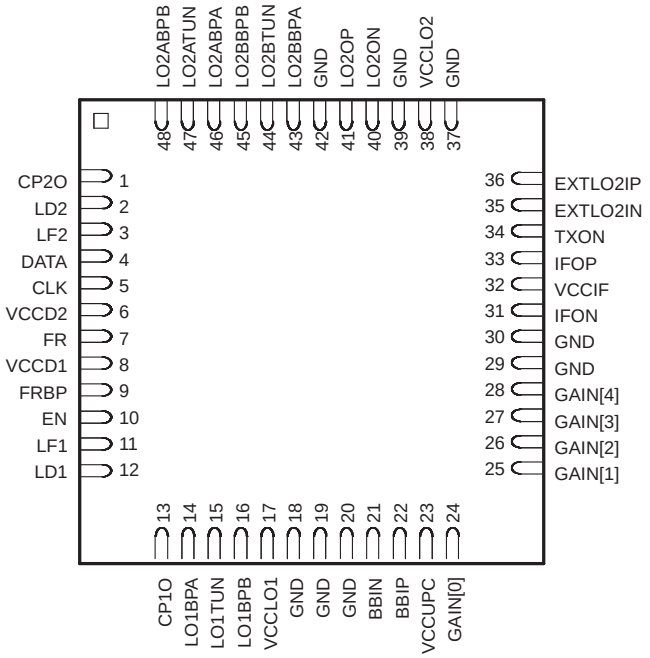
- **Low Phase Noise**
- **Image Reject Upconverter**
- **Dual VCO/PLL For Double Upconversion Architecture**
- **On-Chip VCO, Resonator, and PLL Only; Requires Off-Chip Loop Filter**
- **External S-Band VCO Option**
- **5-Bit Transmit Level Control, 32 dB in 1-dB Steps**
- **S-Band LO Frequency Range:**
  - **TRF1121: 1500 to 2500 MHz**
  - **TRF1221: 1700 to 3600 MHz**
- **UHF LO Frequency Range: 250 MHz to 350 MHz**
- **Input Frequency Range: 10 MHz to 70 MHz**
- **S-Band LO Phase Noise Typical 0.5° rms (100 Hz to 1 MHz)**
- **Output Power Range From –32 dBm to 0 dBm in 1-dB Steps (500-mVpp Differential Input)**
- **Minimum UHF LO Step Size of 50 kHz for TRF1121 and 62.5 kHz for TRF1221**
- **Image Rejection: –50 dBc, Typical (20–40 MHz Tx IF Input)**
- **LO Leakage: –36 dBm, Typical**
- **Third-Order IMD: < –60 dBc at Maximum Gain**

DESCRIPTION

The TRF1121 and TRF1221 are VHF-UHF upconverters with integrated UHF and S-band frequency synthesizers for radio applications in the 2-GHz to 4-GHz range. The IC performs the first upconversion and generates the local oscillator (LO) for the second upconversion. The device uniquely integrates an image reject mixer, IF gain blocks, 5-bit gain control, and two complete phase-locked-loop (PLL) circuits including: VCOs, resonator circuit, varactors, dividers, and phase detectors.

The TRF1121 and TRF1221 are designed to function as part of complete 2.5-GHz and 3.5-GHz radio chipsets, respectively. In the chipset, the transmit chain operates as a double upconverter from an IF frequency input (typically from a baseband modem's DAC) to an RF output frequency. The TRF1121/ TRF1221 performs the first upconversion from IF signals in the range of 10 MHz to 60 MHz to a second IF frequency in the range of 300 MHz to 360 MHz. The radio chipset features sufficient linearity, phase noise, and dynamic range to work in either single carrier or multicarrier, line-of-sight or non-line-of-sight, standard (IEEE 802.16), or proprietary systems. Due to the modular nature of the chipset, it is ideal for use in systems that employ transmit or receive diversity.

LPCC–48 PACKAGE
(TOP VIEW)



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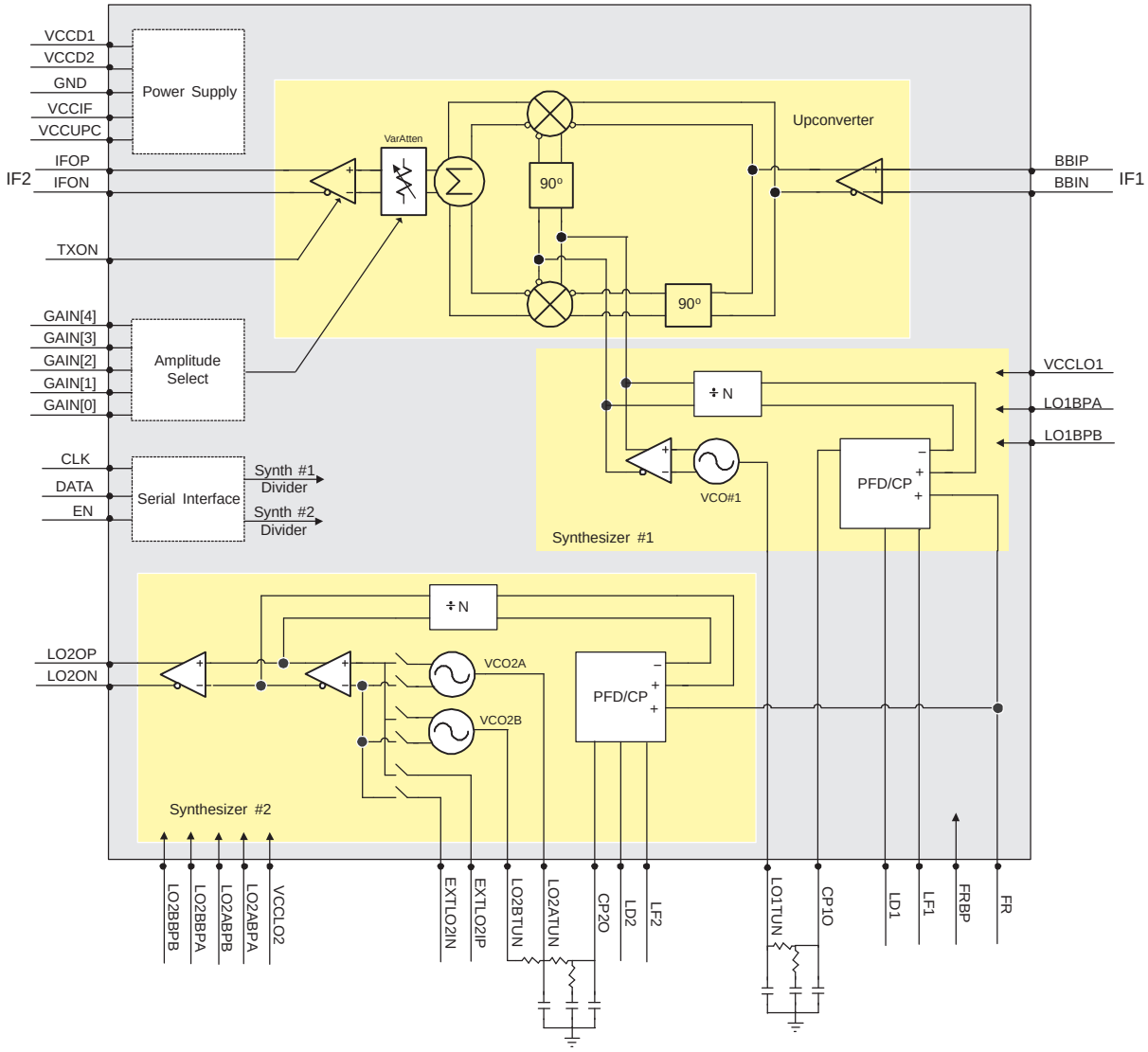
BLOCK DIAGRAM



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TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NAME	NO.			
BBIN	21	I	Analog	Baseband IF input (2-kΩ differential) negative, dc-coupled; internal voltage is 4 V DC
BBIP	22	I	Analog	Baseband IF input (2-kΩ differential) positive, dc-coupled; internal voltage is 4 V DC
CLK	5	I	Digital	Serial interface clock input
CP1O	13	O	Analog	Analog synthesizer 1 charge pump output
CP2O	1	O	Analog	Analog synthesizer 2 charge pump output
DATA	4	I	Digital	Serial interface data input
EN	10	I	Digital	Serial interface load enable (active-high)
EXTLO2IN	35	I	Analog	External input for LO2 (differential) negative and logic level for VCO select.
EXTLO2IP	36	I	Analog	External input for LO2 (differential) positive and logic level for VCO select.
FR	7	I	Analog	18-MHz reference clock input, HCMOS input. (DC level = 2.5 V)
FRBP	9	O	Analog	Reference frequency bypass. Internally biased to 2.5 V.
GAIN[0]	24	I	Digital	Gain control bit 0 (LSB). Logic low induces 1-dB attenuation.
GAIN[1]	25	I	Digital	Gain control bit 1. Logic low induces 2-dB attenuation.
GAIN[2]	26	I	Digital	Gain control bit 2. Logic low induces 4-dB attenuation.
GAIN[3]	27	I	Digital	Gain control bit 3. Logic low induces 8-dB attenuation.
GAIN[4]	28	I	Digital	Gain control bit 4 (MSB). Logic low induces 16-dB attenuation.
GND	18–20, 29, 30, 37, 39, 42		Power	Ground
IFON	31	O	Analog	IF analog output (100-Ω differential) negative, dc-coupled, internal voltage is 2.1 V dc.
IFOP	33	O	Analog	IF analog output (100-Ω differential) positive, dc-coupled, internal voltage is 2.1 V dc.
LD1	12	O	Digital	Synthesizer 1 lock detect output, high is locked.
LD2	2	O	Digital	Synthesizer 2 lock detect output, high is locked.
LF1	11	O	Analog	Lock detect filter capacitor for LO1, 0.01 µF typical 100 kΩ(1)
LF2	3	O	Analog	Lock detect filter capacitor for LO2, 0.01-µF typical, 100-kΩ pullup(1)
LO1BPA	14	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
LO1BPB	16	O	Analog	Bypass capacitor for LO1, 0.1 µF (min), DCV = 1 V
LO1TUN	15	I	Analog	VCO synthesizer 1 tuning port
LO2ABPA	46	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
LO2ABPB	48	O	Analog	Bypass capacitor for LO2A, 0.1 µF (min), DCV = 1 V
LO2ATUN	47	I	Analog	LO2A tune port
LO2BBPA	43	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
LO2BBPB	45	O	Analog	Bypass capacitor for LO2B, 0.1 µF (min), DCV = 1 V
LO2BTUN	44	I	Analog	LO2B tune port
LO2ON	40	O	Analog	LO2 negative output (differential) and positive VCC bias (5 V) for LO buffer amplifier
LO2OP	41	O	Analog	LO2 positive output (differential) and positive VCC bias (5 V) for LO buffer amplifier
TXON	34	I	Digital	IF amplifier enable active high
VCCD1	8	I	Power	5-V power for digital
VCCD2	6	I	Power	5-V power for digital
VCCIF	32	I	Power	5-V power for analog
VCCLO1	17	I	Power	VCC for LO1
VCCLO2	38	I	Power	VCC for LO2 A and B
VCCUPC	23	I	Power	5-V power for analog
Back	Back side of package has metal base that must be grounded for thermal and RF performance			

(1) Current leakage on the order of 10 µA through the capacitor or by any other means from either LF pin can cause false loss-of-lock signals. The two pullup resistors (R16 and R17) in Figure 23 reduce this sensitivity.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	DC supply voltage	0 to 5.5	V
I_{CC}	DC supply current	270	mA
P_{in}	RF input power	20	dBm
T_J	Junction temperature	150	°C
P_{diss}	Power dissipation	1.5	W
	Digital input voltage	–0.3 to V_{CC} + 0.3	V
	Analog input voltage	V_{CC}	V
$R_{\theta JC}$	Thermal resistance, junction-to-ambient(1)	25	°C/W
T_{stg}	Storage temperature	–40 to 105	°C
T_{op}	Operating temperature	–40 to 85	°C
	Lead temperature, 40 seconds maximum	260	°C

(1) Thermal resistance is junction-to-ambient assuming thermal pad with nine thermal vias under package metal base. See the recommended PCB layout.

ELECTRICAL CHARACTERISTICS

The characteristics listed in the following tables are at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

DC CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	T_A = 25°C	4.8		5.2	V
I_{CC_TxON}	Supply current	T_A = 25°C, TXON enabled		180		mA
I_{CC_TxOFF}		T_A = 25°C, TXON disabled		130		

UPCONVERTER CHARACTERISTICS

Input signal 500 mVpp, V_{CC} = 5 V, 25°C, IF1 = 26 MHz, IF2 = 325 MHz unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IF1}	Input center frequency	See Figure 3		26		MHz
f_{IF2}	Output frequency range		270		400	MHz
V_{BB}	Input signal level	Peak-to-peak differential		500	1000	mV
Z_{IF1}	Input IF1 differential impedance			2		kΩ
P_{out}	Output power (maximum gain)	Measured at IF2 (IF2OP, IF2ON) with 500-mVpp differential input to IF1(BBIP, BBIN) and GAIN[4:0] = 11111		0		dBm
	Output power (minimum gain)	Measured at IF2 (IF2OP, IF2ON) with 500-mVpp differential input to IF1(BBIP, BBIN), GAIN[4:0] = 00000		–32		dBm
ΔG_{max}	Gain flatness	300 MHz < IF2 < 330 MHz		±0.3		dB
ΔP_{STEP}	Gain step size		0.7	1	1.3	dB
OP1dB	Output power a 1-dB gain compression	GAIN[4:0] = 11111		12		dBm
OIP3	Output third order intercept	For any gain setting		24		dBm
IR	Image rejection	IF1 = 15 to 45 MHz			–30	dBc
P_{LO1}	LO1 leakage	At GAIN[4:0] = 11111 decreases dB for dB as gain state is changed		–36		dBm
NF	Input noise figure	At max gain (GAIN[4:0] = 11111), no worse than 1-dB degradation per 1 dB of attenuation		27		dB
Z_{IF2}	Output RF impedance	Differential		100		Ω

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SYNTHESIZER #1 (UHF-BAND PLL) CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency			18		MHz
f_{VCO1}	Frequency	TRF1121 and TRF1221	250		350	MHz
$\phi_{nFRVCO1}$	Free-running VO1 SSB phase noise at 100 kHz			–115		dBc/Hz
$\phi_{nLD\ LO1}$	Locked synthesizer-1 SSB phase noise at 10 kHz			–115		dBc/Hz
$\phi_{nLD\ LO1}$	Locked synthesizer-1 SSB phase noise at 100 kHz			–115		dBc/Hz
$f_{LD\ LO1}$	Locked synthesizer-1 integrated RMS phase noise	100 Hz to 1 MHz			0.2	°
MS_{LO1}	Tuning sensitivity	For V_{LO1TUN} > 2 V	30		60	MHz/V
Δf_{LO1}	Step size	TRF1121, 18-MHz reference input	50			kHz
		TRF1221, 18-MHz reference input	62.5			
$R_{RS\ LO1}$	Reference spur rejection		–70			dBc
$R_{FS\ LO1}$	Fractional spurs rejection			–60		dBc

SYNTHESIZER #2 (S-BAND PLL) CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency			18		MHz
f_{LO2A}	Output frequency, VCO2A	TRF1121	1500		2100	MHz
		TRF1221	1700		2450	
f_{LO2B}	Output frequency, VCO2B	TRF1121	1700		2500	MHz
		TRF1221	2400		3600	
MS_{LO2A}	Tuning sensitivity, VCO2A	TRF1121 For VLO1TUN >2 V	150		350	MHz/V
		TRF1221 For VLO1TUN >2 V	200		400	
MS_{LO2B}	Tuning sensitivity, VCO2B	TRF1121 For VLO1TUN >2 V	200		400	MHz/V
		TRF1221 For VLO1TUN >2 V	350		550	
Δf_{LO2}	Step size	For 18-MHz reference input	1			MHz
P_{LO2}	Output power level	Measured into a 100-Ω differential load at the LO1OP/N port		–3		dBm
$\phi_{nFR\ VCO2}$	Free-running SSB phase noise at 100 kHz	Measured into a 100-Ω differential load at the LO1OP/N port		–100		dBc/Hz
$\phi_{nLD\ LO2}$	Locked synthesizer SSB phase noise at 10 kHz	Measured into a 100-Ω differential load at the LO2OP/N port with loop filter set to 400 kHz nominal		–102	–97	dBc/Hz
	Locked synthesizer SSB phase noise at 100 kHz			–100	–95	
$\phi_{LD\ LO2}$	Integrated RMS phase noise	Locked, 100 Hz to 1 MHz		0.5	1	°
$R_{RS\ LO2}$	Reference sideband suppression	Measured into a 100-Ω differential load at the LO1OP/N port. PLL loop bandwidth ~400 kHz		–65	–60	dBc
$R_{FS\ LO2}$	Fractional spur suppression	At 1 MHz offset (Loop BW ~400 kHz)		–50	–45	dBc
		At 2 MHz offset (Loop BW ~400 kHz)		–65	–60	
		All others		–70	–70	
$R_{H\ LO2}$	Harmonics suppression	Measured into a 100-Ω differential load at the LO1OP/N port			–20	dBc
RL_{LO2}	Output return loss	Measured into a 100-Ω differential load at the LO1OP/N port	–11	–16		dB
P_{extVCO}	Ext VCO input power			–13		dBm
RL_{extVCO}	Ext VCO port input return loss	Differential mode	–10	–15		dB
$Z_{in\ extVCO}$	Ext VCO port input impedance	Differential mode		100		Ω

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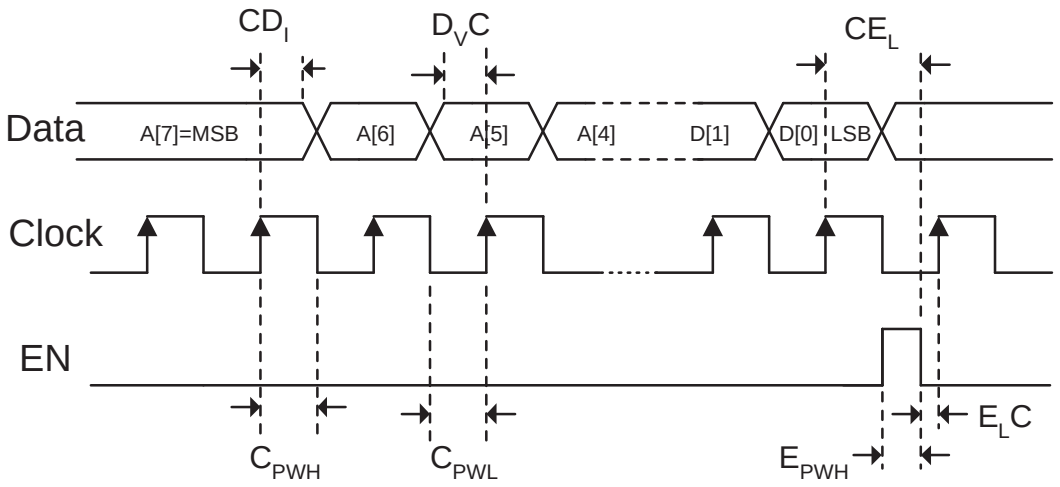
INPUT REFERENCE REQUIREMENTS

Conditions: Signal BW = 6 MHz nom, 15 dB maximum loss IF2 SAW filter. See Figure 19

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency			18		MHz
	Temperature stability	Customer requirements				PPM
V_{FR}	Ref. source input voltage (1)	HCMOS output	4	4.5	5	Vpp
DC_{fref}	Reference input symmetry	Waveform duty cycle	40%		60%	
t_{FR}	Reference source pulse rise time	10% to 90% of maximum voltage transition		1	4	ns
f_{FR}	Reference phase noise at 10-kΩ offset			–153	–150	dBc/Hz

(1) Note that for source peak-to-peak voltages of less than 4 V and dc component other than 2.5 V, degradation of the close-in phase noise may occur. For oscillators with no dc component, a dc voltage may be applied using a voltage divider (see the schematic, Figure 23).

AC TIMING, SERIAL BUS INTERFACE



PARAMETER		MIN	TYP	MAX	UNIT
CD_I	Clock to data invalid	10			ns
D_VC	Data valid to clock	10			ns
C_{PWH}	Clock pulse duration high	50			ns
C_{PWL}	Clock pulse duration low	50			ns
CE_L	Clock to enable low	10			ns
E_LC	Enable low to clock	10			ns
E_{PWH}	Enable pulse duration	10			ns

Figure 1. Serial Interface Timing Diagram

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DIGITAL INTERFACE CHARACTERISTICS

Conditions: Signal BW = 6 MHz nom, 15 dB maximum loss IF2 SAW filter. See Figure 19

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		2.1		5	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current		0		50	µA
I_{IL}	Input low current		0		–50	µA
C_I	Input capacitance			3		pF
V_{OH}	Output logic 1 voltage	0 to 100-µA load	2.4		3.6	V
R_{OH}	Output logic 1 impedance			18		kΩ
V_{OL}	Output low voltage	0 to –100-µA load	0		0.4	V

AUXILIARY AND CONTROL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXON	IF amplifier enable	IF output on		High		
		IF output off		Low		
EXTLO2IP	On-chip VCO2A selection	Logic level applied to EXTLOIP and EXTLOIN pins to select either on chip VCO 2A or 2B. Pullup resistor = 200 Ω and pulldown resistor = 1 kΩ.		High		
EXTLO2IN				Low		
EXTLO2IP	On-chip VCO2B selection			Low		
EXTLO2IN				High		
EXTLO2IP	On-chip VCO2 selection	Logic level applied to EXTLOIP and EXTLOIN pins to select the external VCO2 input		Low		
EXTLO2IN				Low		

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FREQUENCY PLAN

The TRF1121 and TRF1221 allow a variety of frequency plans. Figure 2 illustrates the allowable combinations of first and second IFs. However, due to the fact that the chip features image reject mixers, significant changes in the frequency plan can result in degradation of the image rejection as shown in Figure 3. LO leakage vs LO1 frequency is shown in Figure 4.

In order to maintain maximum image rejection and LO suppression, a recommended frequency plan is TxIF1 = 26 MHz, TxIF2 = 325 MHz.

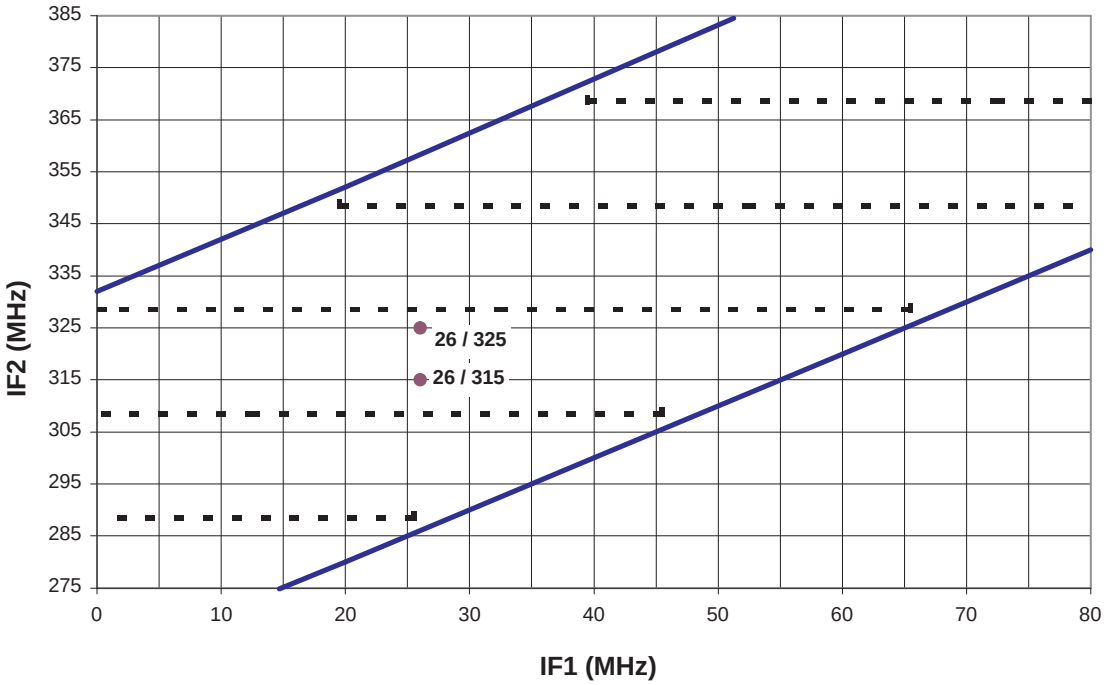

Figure 2. Potential IF Combinations (TRF1121/1221)

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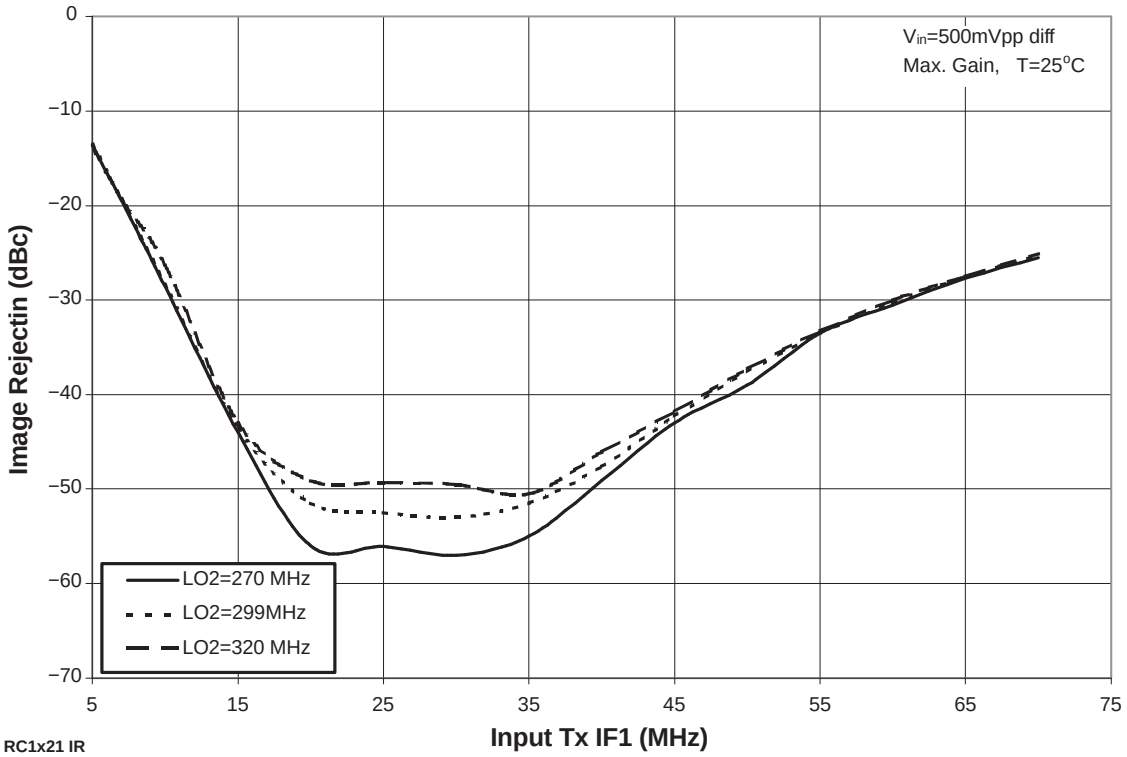

Figure 3. Image Rejection vs IF1, Transmit Chain

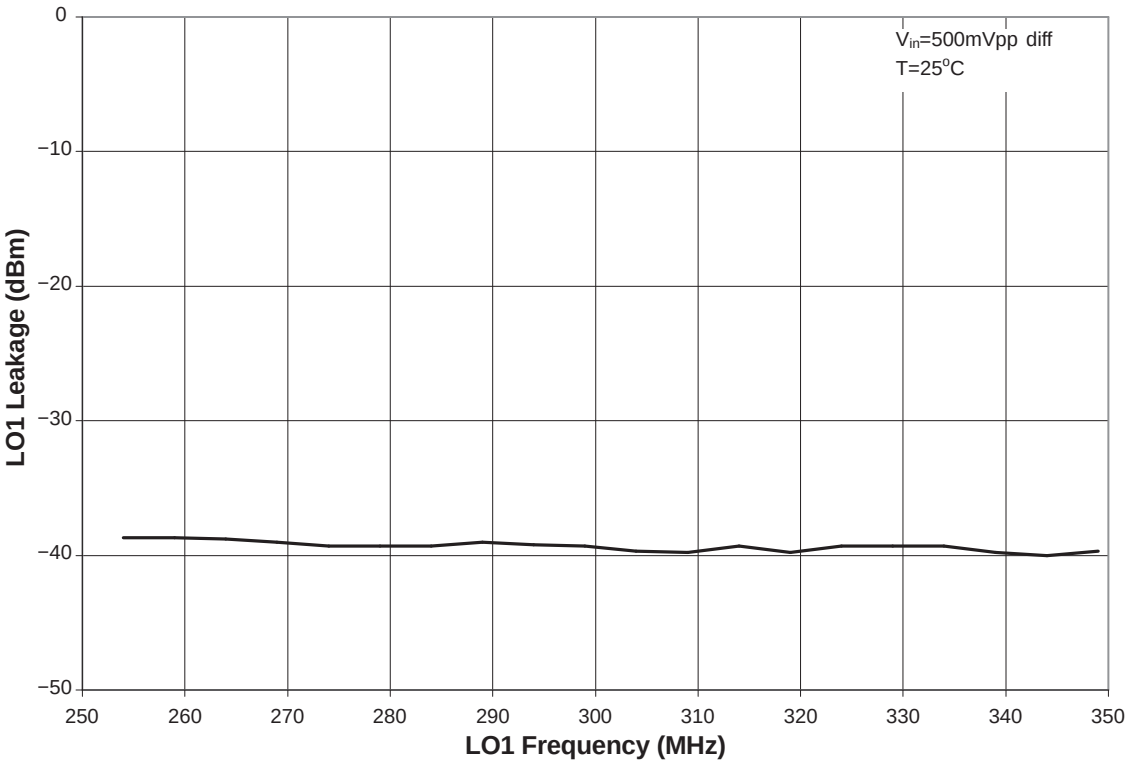

Figure 4. LO1 Leakage at IF2 Port, Maximum Gain

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TRANSMIT LEVEL CONTROL

The TRF1121 and TRF1221 offer 32 dB of gain control through a five-wire parallel bus. When driven with a 500-mVpp differential baseband IF signal, the transmit level can be programmed between –32 dBm and 0 dBm in 1-dB steps.

Figure 5 shows the output power, two-tone imtermodulation level, LO leakage, and gain deviation from ideal vs gain state, while Figure 6 shows the upconverter gain variation vs temperature.

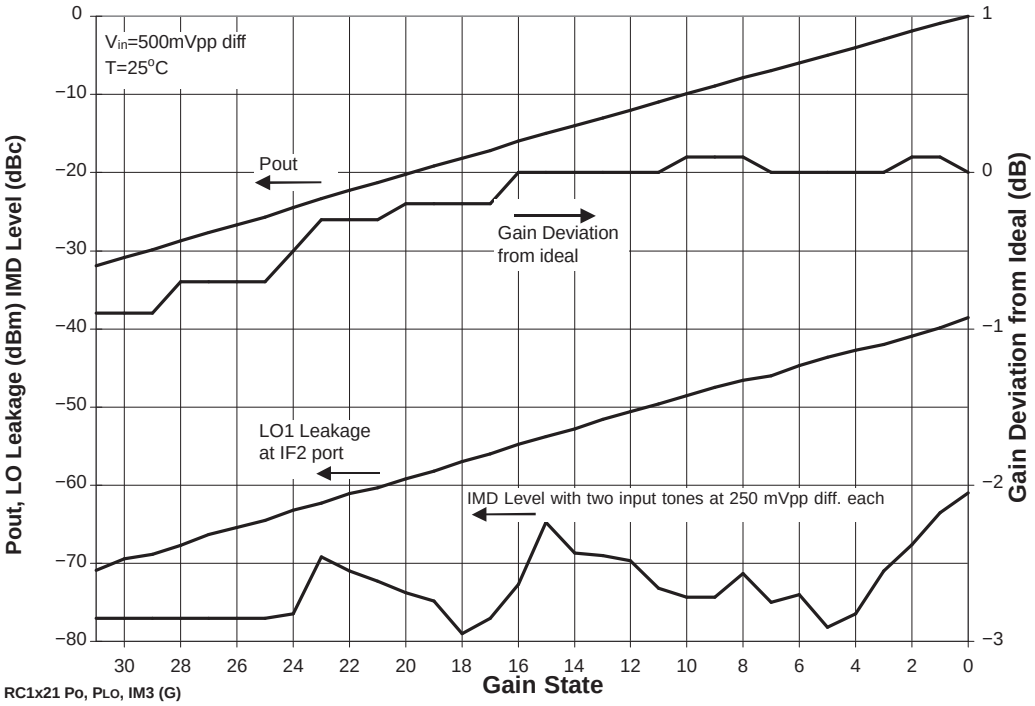

Figure 5. Output Power, LO Leakage and IMD Level vs Gain State

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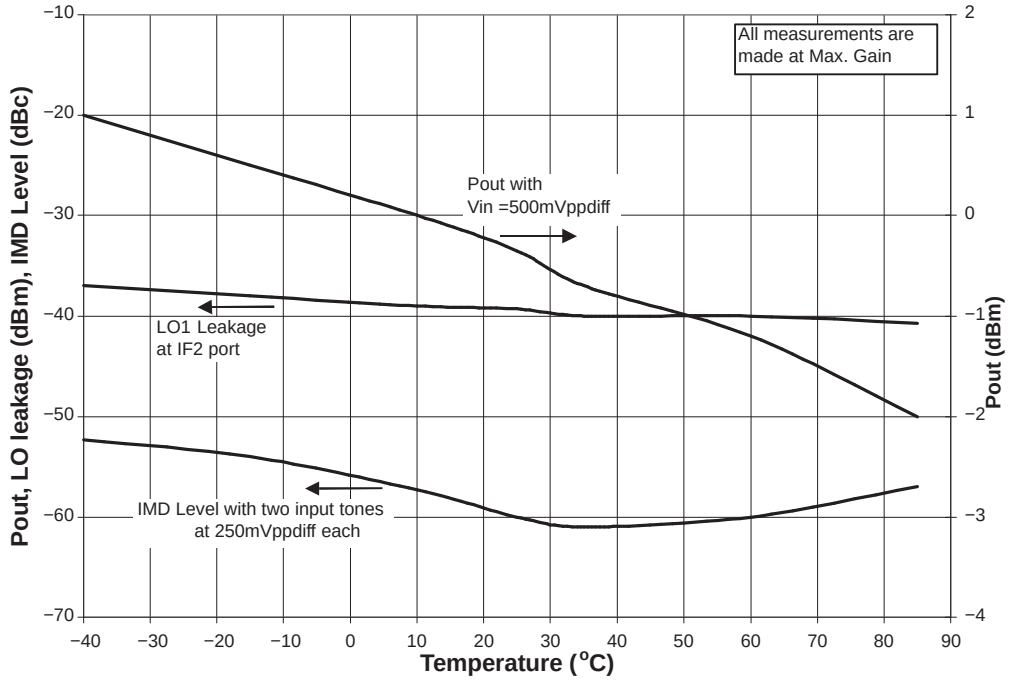
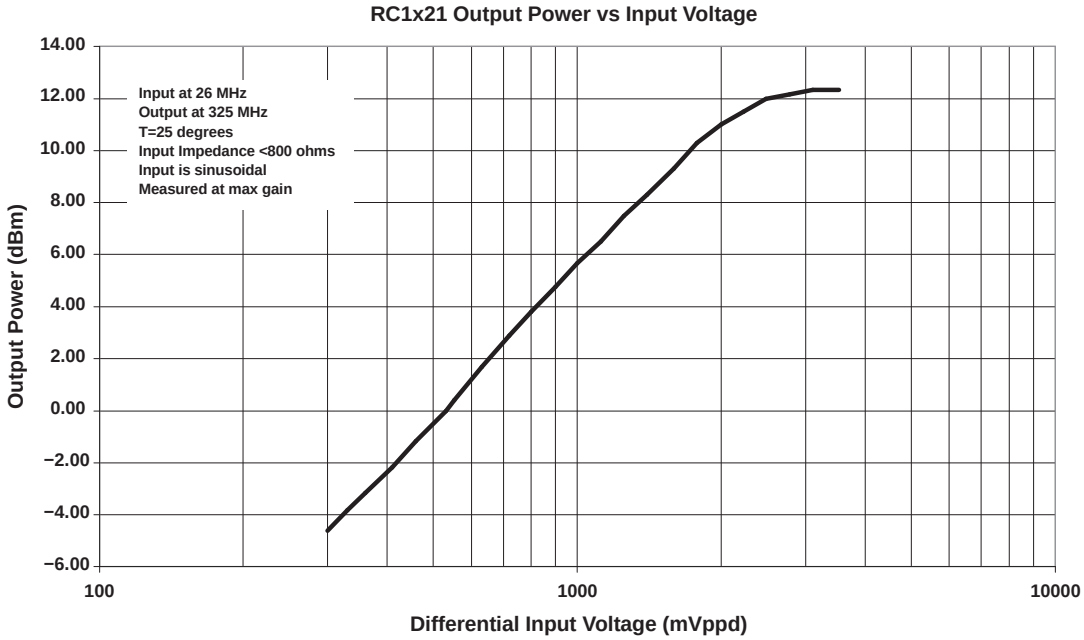


Figure 6. Power Level, IMD and LO1 Leakage Variation vs Temperature at Maximum Gain Setting



NOTE: If left unconnected, the GAIN[0], GAIN[1], GAIN[2], GAIN[3], GAIN[4], and TXEN pins rest on logic-low.

Figure 7. Output Power vs Input Voltage

INTEGRATED SYNTHESIZERS

PLL Programming

Synthesizer #1 (UHF) and synthesizer #2 (S-band) are both integrated in the TRF1121/TRF1221. These two PLLs can be programmed via a 3-wire serial bus (CLK, DATA, and EN) from the baseband processor. The timing specifications are given in the ac timing table.

Synthesizer #2 has a step size of 1 MHz, while Synthesizer #1 offers a step size of 50 kHz, both assuming an 18-MHz reference frequency. Different reference frequencies yield different step sizes, many of which may be non-integer.

NOTE:

If left unconnected, the DATA, CLK and EN pins rest on logic-high. EN is level-sensitive.

Data is written to the PLLs according to the format in Figure 8.

MSB			Byte 1				LSB	MSB			Byte 2				LSB	MSB			Byte 3				LSB
Address								Data															
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	0	0	0	0	0	0	0	0	0	Synth #1 N divider						Synth #1 S counter			Synth #1 F counter				
1	0	0	0	0	0	0	1	0	0	Synth #2 N divider						Synth #2 S counter			Synth #2 F counter				
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	PS	0	0	0	0	0	0	0	0
all other addresses reserved for future expansion																							

Figure 8. Serial Interface Data Format

The first eight bits are the appropriate address for the instruction set and the remaining 16 bits are the instructions. The data is 24 bits long (3 bytes). Byte 1 is the address with A[7] being the MSB and A[0] being the LSB. Byte 2 and 3 program the IC with synthesizer information and PS (Polarity Select Bit) information. D[15] is the MSB and D[8] the LSB. The PS bit selects which edge of the reference is used for frequency comparison. Improved spurious and phase noise is achieved by selecting the edge with the fastest rise or fall time. If PS = 1 the rising edge is used as the reference. If PS = 0, the falling edge is used.

The data of Figure 8 must be sent to the TRF1121 / TRF1221 to fully program synthesizers #1 and #2 and the PS bit. Once the synthesizers and the PS bit are fully programmed, the clock signal should be turned off to eliminate any clock-related spurious signals.

The LO1 (UHF oscillator) frequency of oscillation is set by Equation 1:

$$f_{out} = REFIN \times \left[8 \times (N+3) - S - \frac{F}{18} \right] \div \left[2 \times M \right] \quad (1)$$

where:

F = synthesizer F counter

M = 10 for TRF1121 and 8 for 1221

N = synthesizer N divider

S = synthesizer S counter (see Figure 8)

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The TRF1121/TRF1221 contains two independent S-band VCOs and resonator circuits to provide additional frequency range from one IC, however only one VCO can be enabled at a time. These two VCOs are referred to as VCO2A and VCO2B (see the block diagram). The S-band PLL (LO2A or LO2B) frequency of oscillation is set by the following equation:

$$f_{out} = REFIN \times \left[8 \times (N + 3) - S - \frac{F}{18} \right] \quad (2)$$

where:

F = synthesizer F counter

N = synthesizer N divider

S = synthesizer S counter (see Figure 8)

F has a range of 0 to 17. Both N and S have ranges that are limited more by the LO range than by their digital count.

Both synthesizers have a fractional architecture, which allows a high comparison frequency relative to the step size. The S-band PLL operates at a reference frequency of 18 MHz with a minimum phase accumulator frequency of 1 MHz. The UHF PLL operates at a 9-MHz reference with a minimum phase accumulator frequency of 0.5 MHz. The S-band PLL has a step size of 1 MHz and the UHF PLL has a step size of 50 kHz (TRF1121) or 62.5 kHz (TRF1221), when using an 18-MHz reference frequency. Different reference frequencies yield different step sizes, many of which are non-integer. If a different reference frequency is chosen, the step size is linearly related to the step size for 18 MHz.

Step size = step size at 18 MHz $\times$ [REF FREQ / 18 MHz]

In addition to the normal reference spurious signals at the comparison frequency, fractional synthesizers have fractional spurs. The fractional spurs occur at an offset from the LO signal that is dependent on the difference between the LO frequency and integer multiples of the reference frequency. They occur on both sides of the LO carrier. The spur locations can be found by the following process: divide the LO frequency by the reference frequency, take the remainder (fraction to the right of the whole number) and multiply it by the reference frequency. This frequency is the difference between the actual LO frequency and an integer-multiple of the reference frequency. Fractional spurs occur at this frequency and the reference frequency minus this frequency.

The following example best explains the process: if LO2 is set to 2206 MHz when using an 18-MHz reference frequency, then 2206/18 is 122.55556. The difference between the LO and 122 $\times$ 18 MHz is:

0.55556 $\times$ 18 MHz = 10 MHz

The fractional spurs occur at this frequency offset (10 MHz) from LO2 and:

18–10 MHz or 8 MHz offset from LO2.

The fractional spurious level varies with the offset from the LO because the spurs are attenuated by the loop filter response. The larger the offset from the LO, the lower the spur level. In general, spurs at offsets greater than 3 MHz or 4 MHz are below –75 dBc and are not a concern. The worst fractional spur levels occur when they are located at 1-MHz offsets from the LO2. (Note: the fractional spurs are offset from the LO2 by 1 MHz when the difference between the LO2 and an integer multiple of the reference frequency is 1 MHz or 17 MHz).

Although both synthesizers have fractional spurs, for most applications the spurious signals from the UHF synthesizer can be ignored because the LO1 spurs are filtered by the IF2 filter and attenuated by frequency dividers that are located after the LO1 generation. In some frequency plans it is possible to offset LO1 and LO2 to avoid worst case fractional spurs (at 1-MHz offsets) on LO2.

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VCO Tuning Characteristics

The TRF1121 and TRF1221 have internal VCOs with the following frequency vs tuning voltage characteristics.

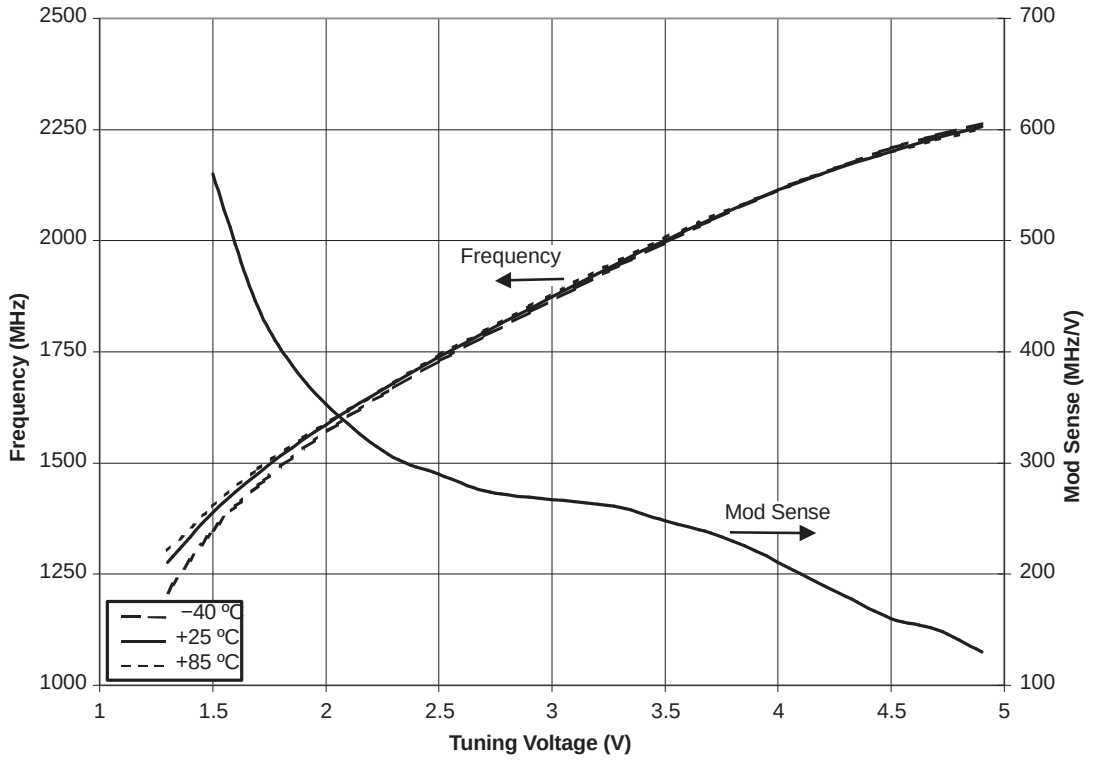

Figure 9. TRF1121 LO2A Frequency LO2ATUN Voltage

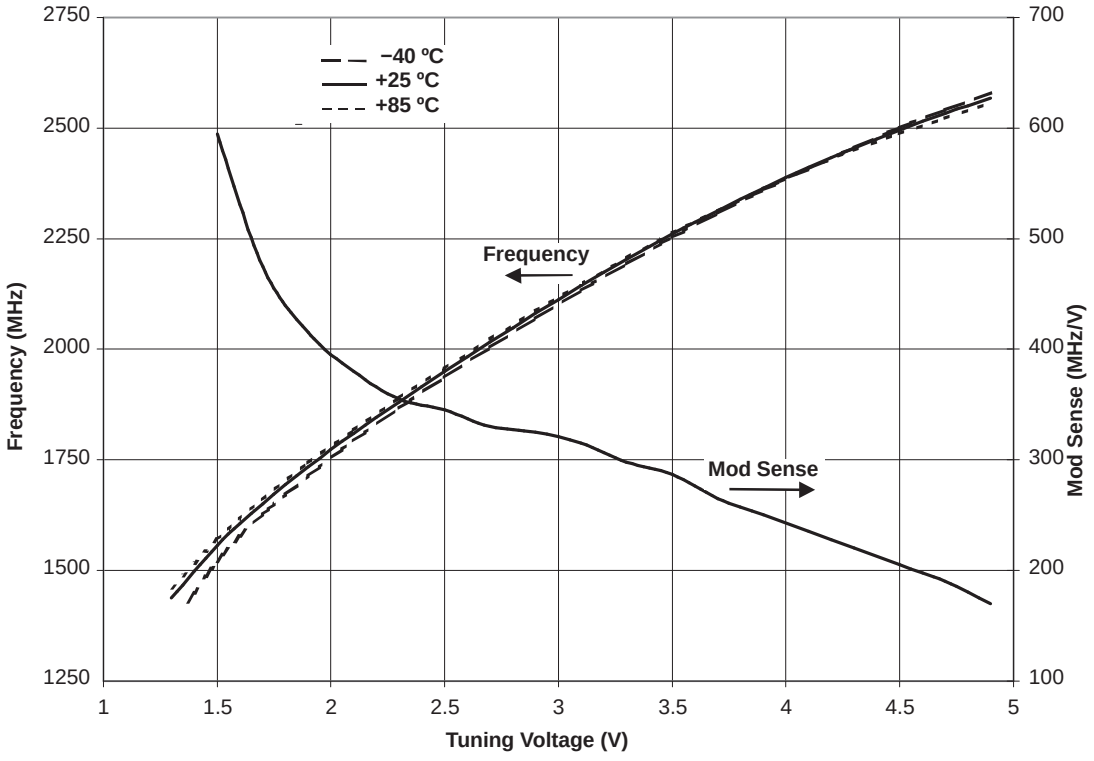

Figure 10. TRF1121 LO2B Frequency vs LO2BTUN Voltage

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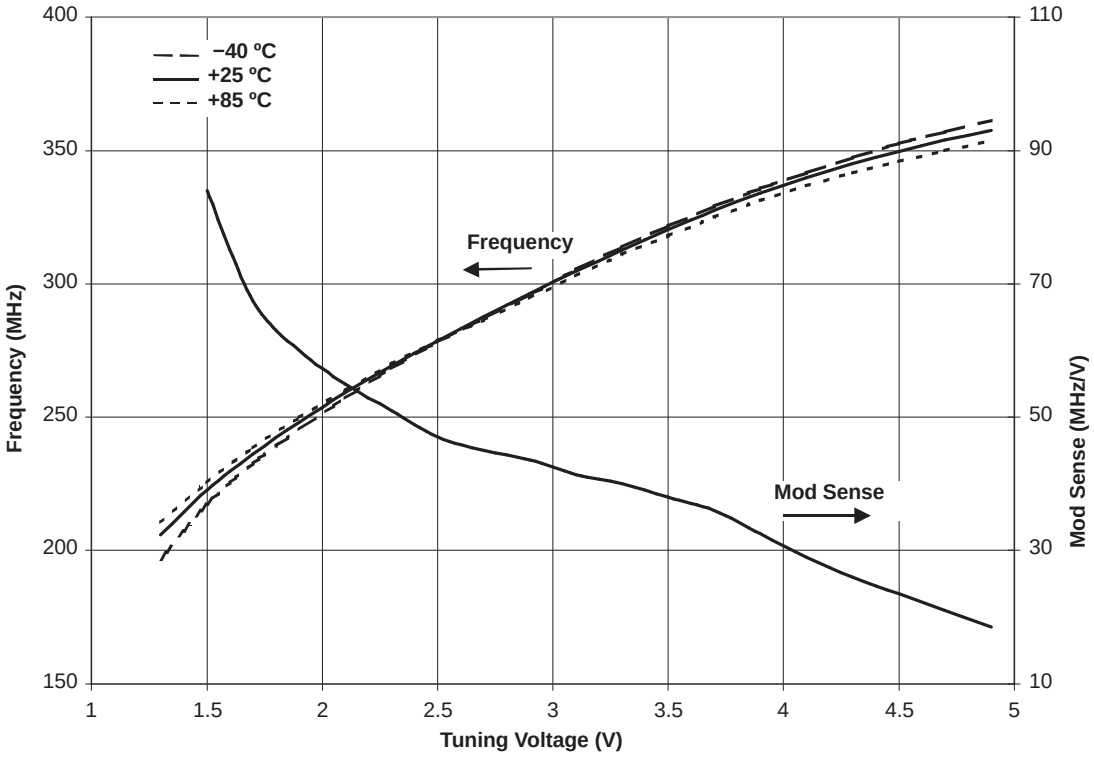

Figure 11. TRF1121 LO1 Frequency vs LO1TUN Voltage

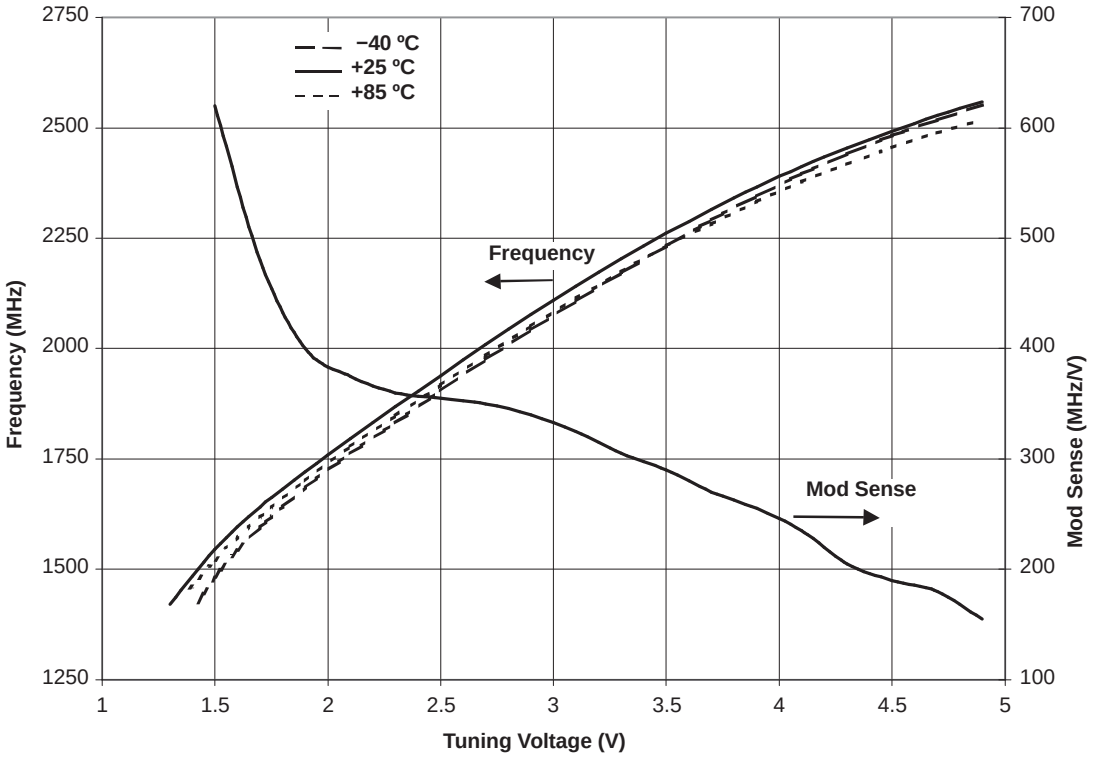

Figure 12. TRF1221 LO2A Frequency vs LO2ATUN Voltage

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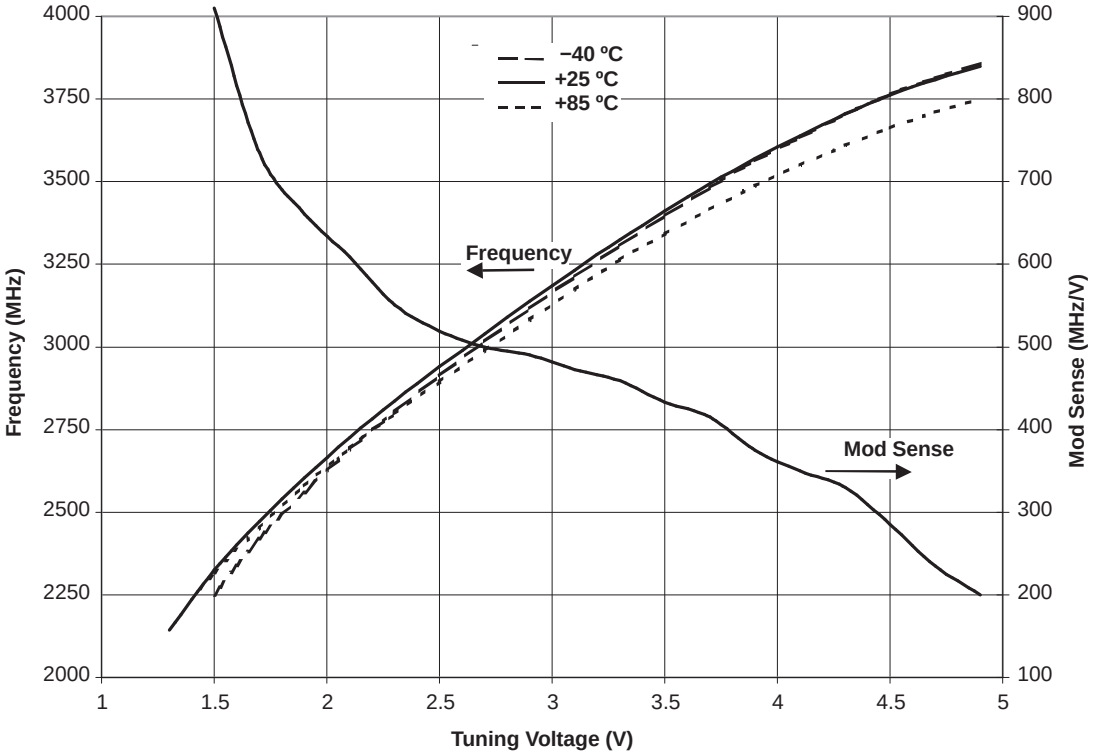

Figure 13. TRF1221 LO2B Frequency vs LO2BTUN Voltage

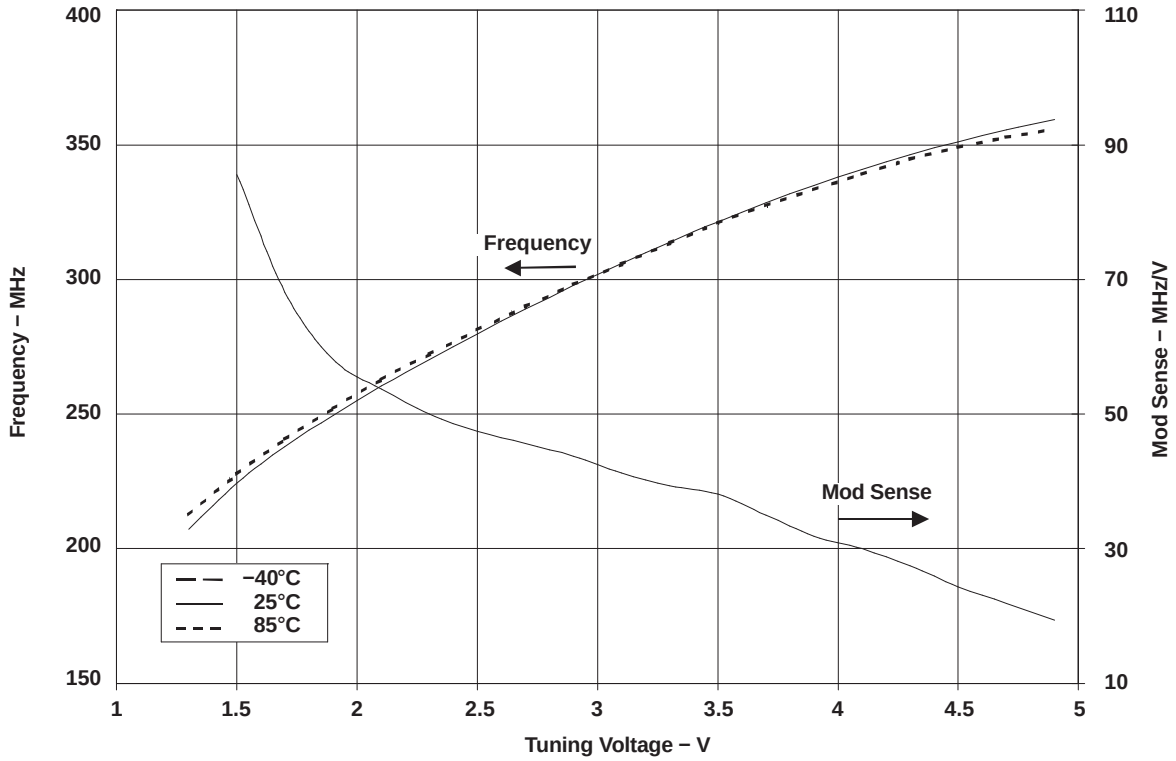

Figure 14. TRF1221 LO1 Frequency vs LO1TUN Voltage

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Phase Noise

The TRF1121 and TRF1221 achieve superior phase noise performance with on-chip resonators and varactors. It is designed to meet the phase noise requirements of both single-carrier and multicarrier systems. Due to the chip architecture, the phase noise and spurious performance of the LO1 PLL is about 15 dB better than the LO2 PLL. The typical phase noise of the TRF1121 and TRF1221 S-band PLL (LO2) with the PLL locked is shown in Figure 15 and Figure 16, respectively. The phase noise plots of the TRF1221 S-band PLL at the min and max range are shown in Figure 20 and Figure 21, respectively. These plots were taken at room temperature and typical voltage conditions.

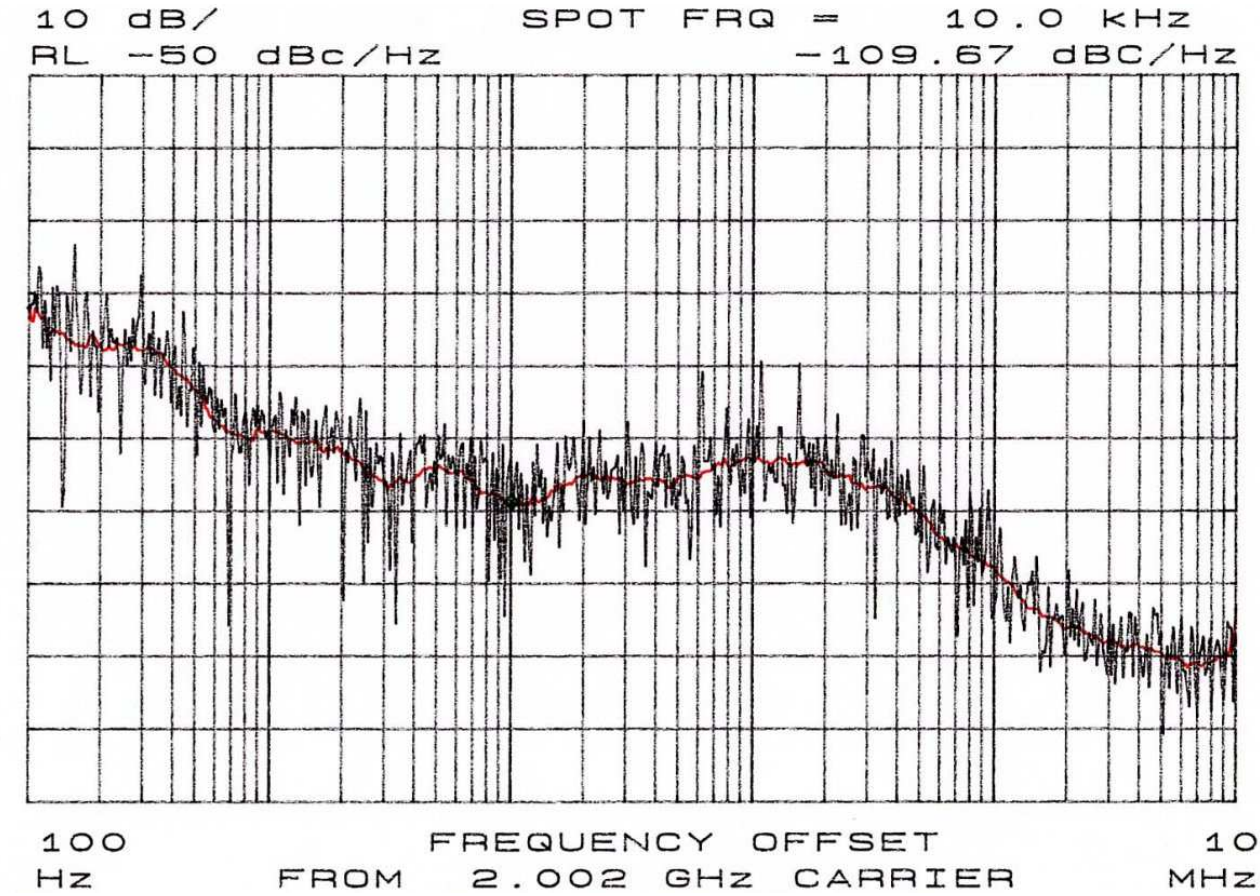

Figure 15. TRF1121 Typical Integrated LO1 (S-Band) Phase Noise is 0.35° rms (100 Hz to 1 MHz)

When designing full-duplex radios that employ narrow T-to-R spacing, one must consider the impact of wide-band phase noise because it can degrade Rx sensitivity. Figure 17 shows typical wide-band composite phase noise performance of the combination of the two integrated PLLs. At 50-MHz offset, typical performance is –145 dBc/Hz.

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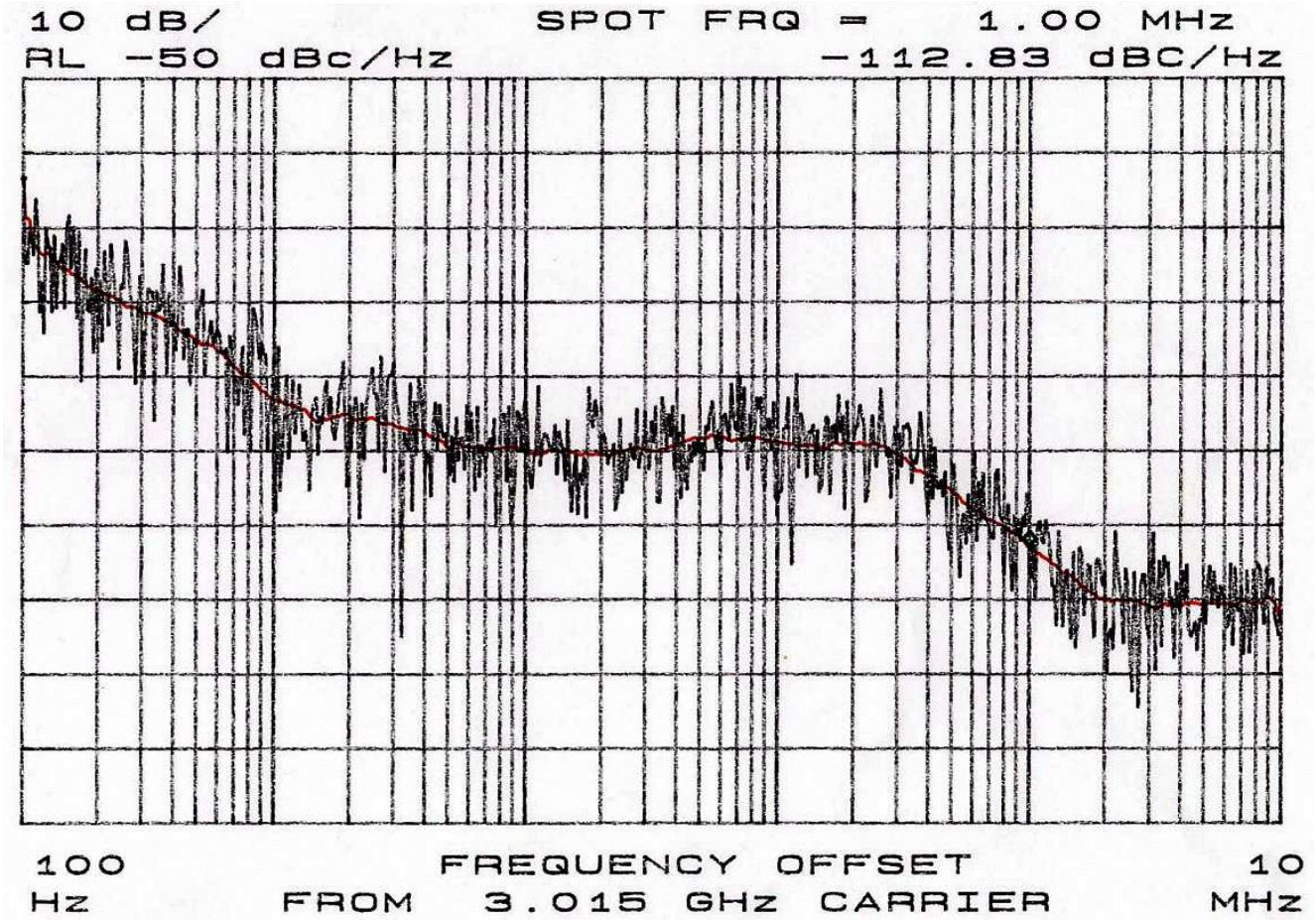

Figure 16. TRF1221 Typical Integrated LO2 (S-Band) Phase Noise is 0.65° rms (100 Hz to 1 MHz)

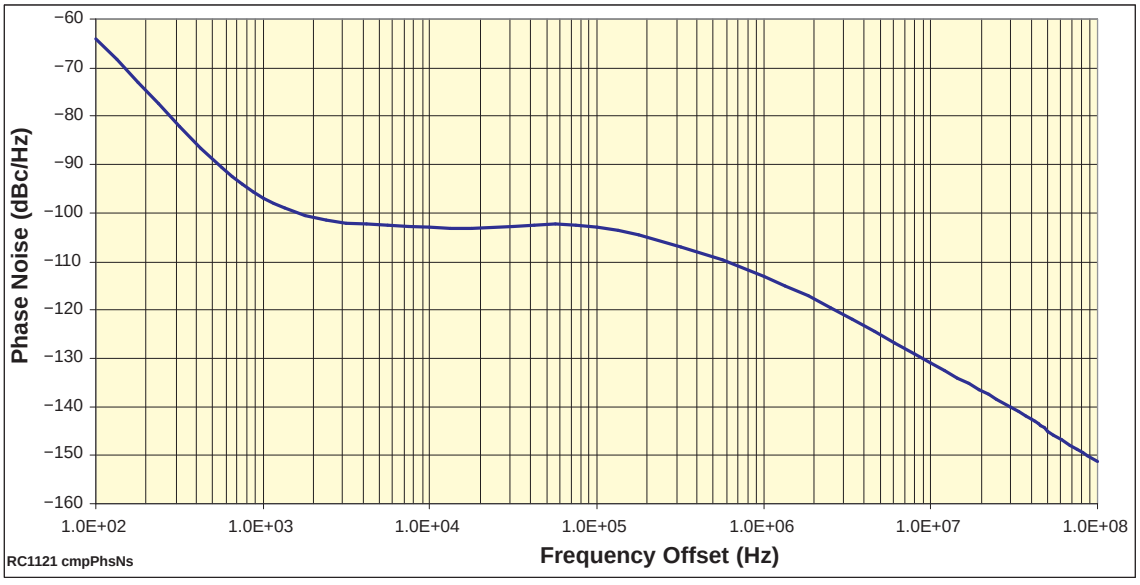

Figure 17. TRF1121 Typical Wide-Band Composite PLL Phase Noise Profile

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Figure 18 shows reference spurs of the S-band (LO2) locked synthesizer and Figure 19 shows the fractional spurs of the same LO at 2-MHz offset from the carrier.

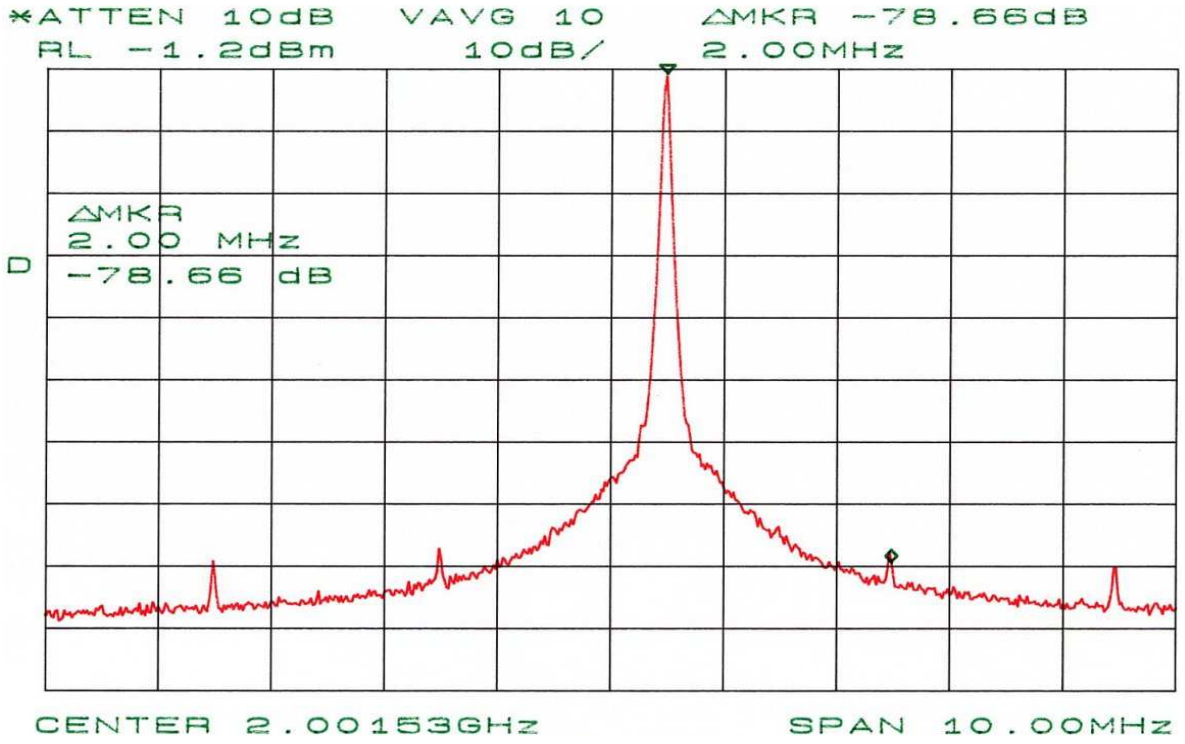

Figure 18. TRF1121 Reference Spurs on LO2 Output

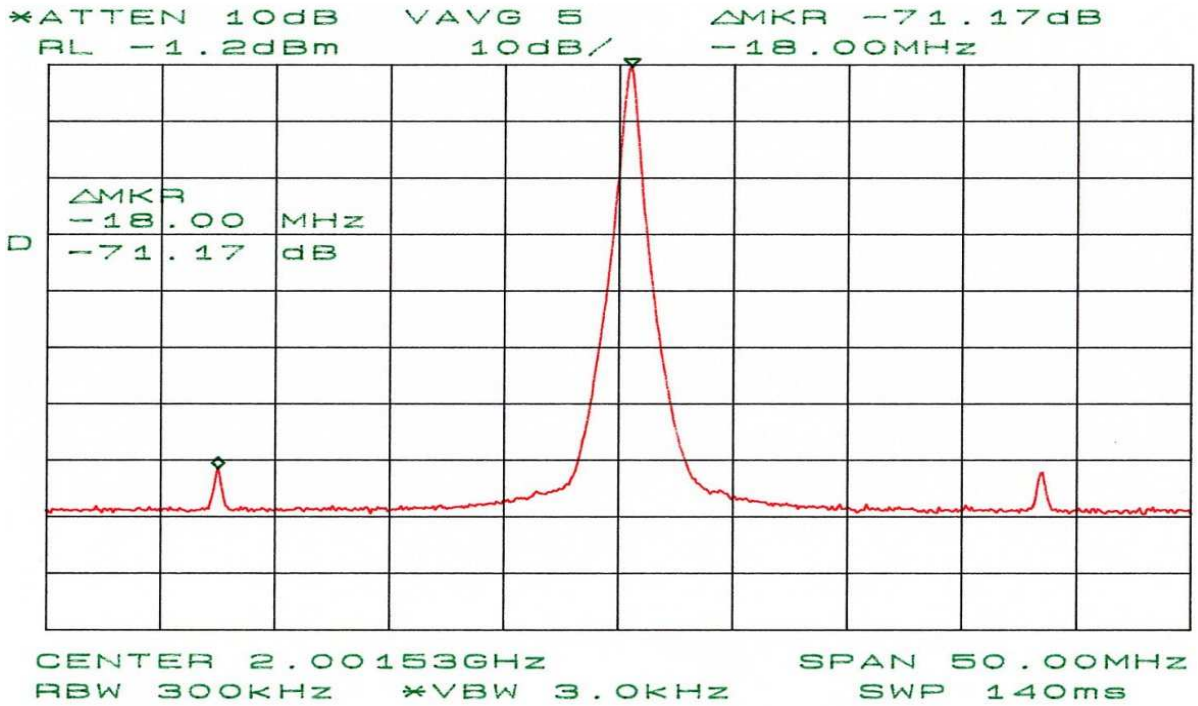

Figure 19. TRF1121 Fractional Spurs on LO2 (2-MHz Offset)

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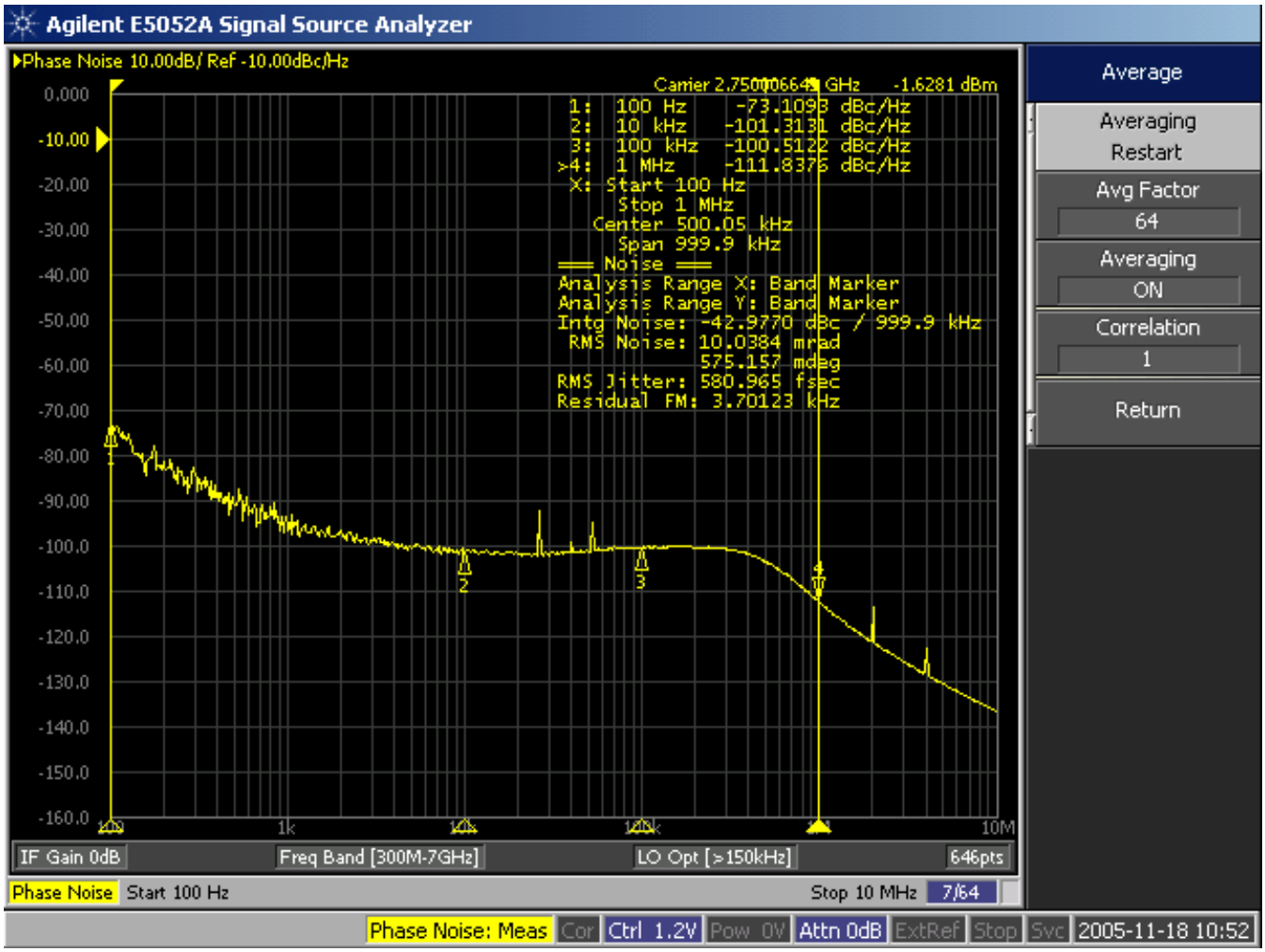

Figure 20. Phase Noise - 2750 MHz

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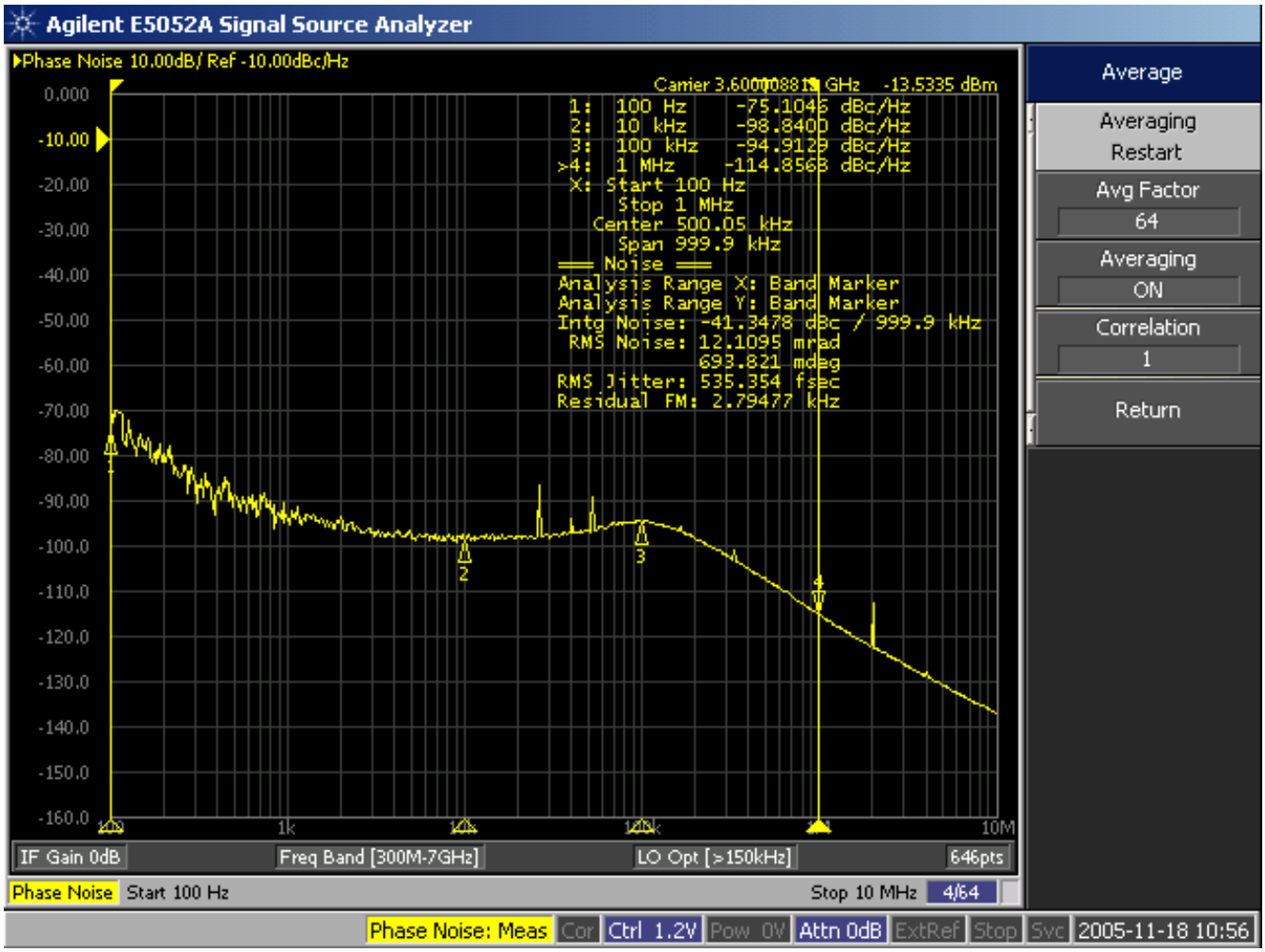

Figure 21. Phase Noise - 3600 MHz

For systems that demand tighter phase noise performance than that offered by Texas Instruments internal VCOs, a provision exists for connection of an external VCO. Texas Instruments PLL still locks the VCO to the reference frequency, and the ASIC provides an external tuning voltage that drives the VCO.

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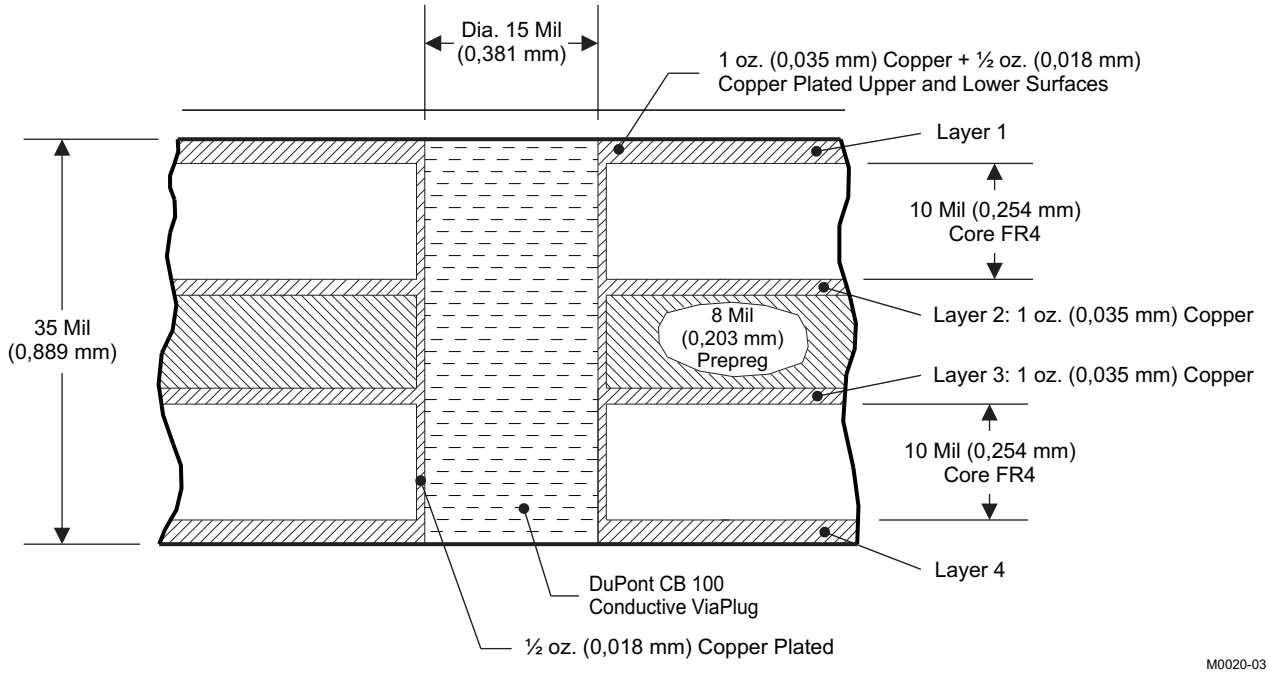
APPLICATION INFORMATION

A typical application schematic is shown in Figure 23.

The recommended PCB layout mask is shown in Figure 24. PCB material recommendations are shown in Table 1 and Figure 22.

Table 1. PCB Recommendations

Board material	FR4
Board material core thickness	10 mil (0.254 mm)
Copper thickness (starting)	1 oz (0.035 mm)
Prepreg thickness	8 mil (0.203 mm)
Recommended number of layers	4
Via plating thickness	0.5 oz (0.018 mm)
Final plate	White immersion tin
Final board thickness	33 mil–37 mil (0.838 mm–0.94 mm)



NOTE: Top and bottom surface finish: copper flash with 50-µinch to 70-µinch (1.27-µm to 1.78-µm) white immersion tin

Figure 22. PCB Construction and Via Cross Section

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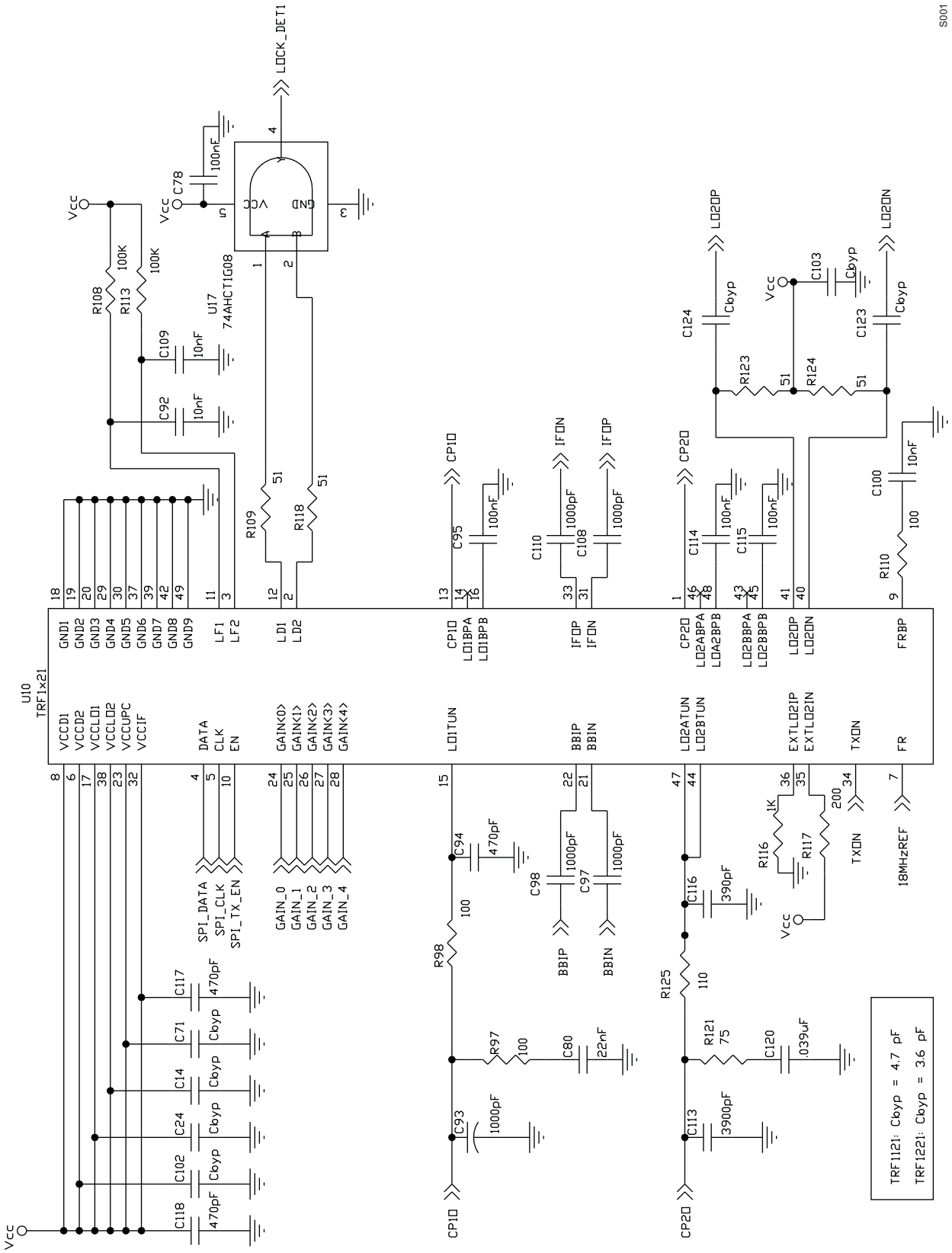
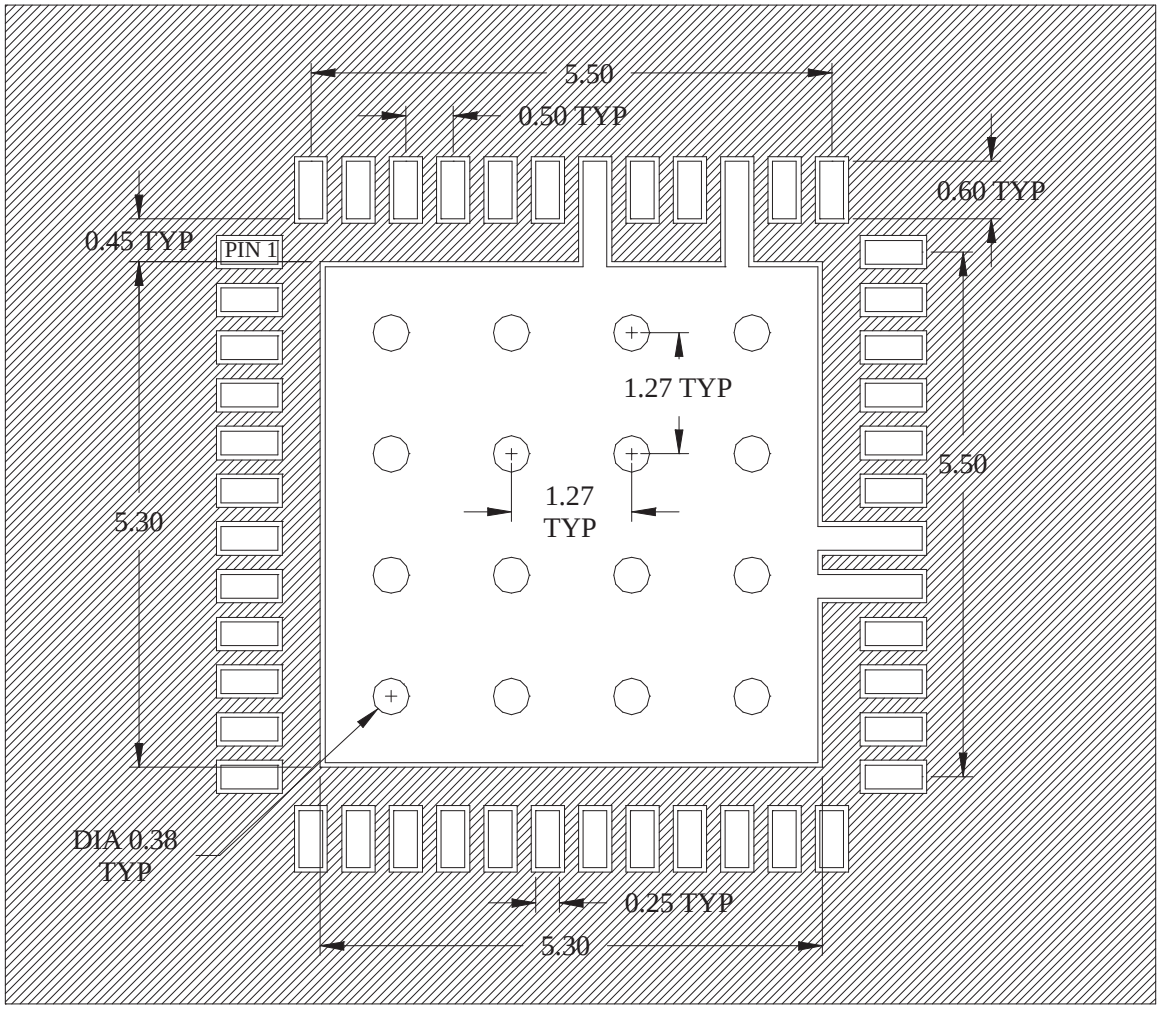


Figure 23. Typical Application Schematic



SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

16 VIA HOLES, EACH 0.38 mm.

DIMENSIONS in mm

Figure 24. PCB Layout Mask for TRF1121/TRF1221

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1121IRGZR	NRND	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85	TRF 1121	
TRF1121IRGZRG3	NRND	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85	TRF 1121	
TRF1121IRGZT	NRND	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1121	
TRF1121IRGZTG3	NRND	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1121	
TRF1221IRGZR	NRND	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1221	
TRF1221IRGZRG3	NRND	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1221	
TRF1221IRGZT	NRND	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85	TRF 1221	
TRF1221IRGZTG3	NRND	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85	TRF 1221	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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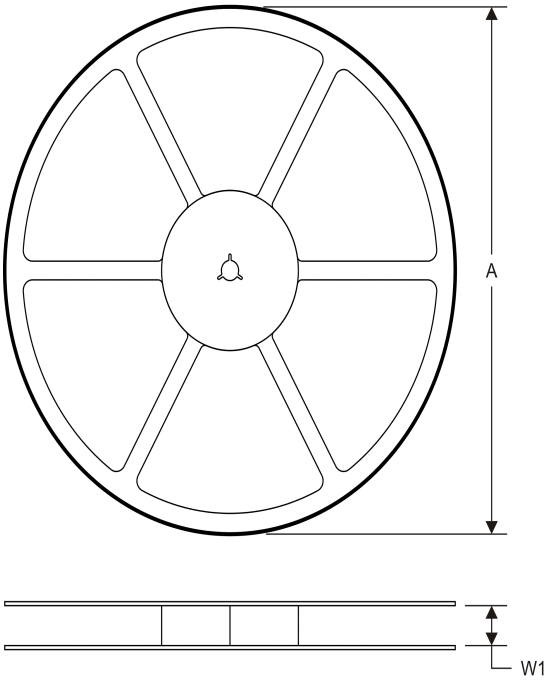
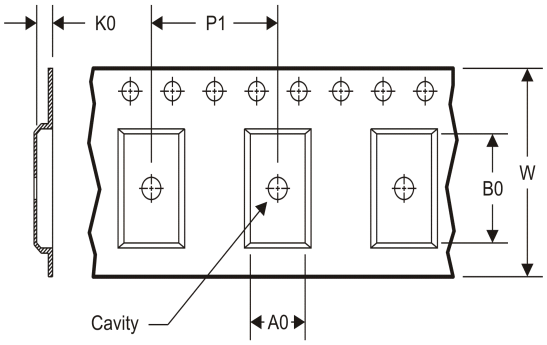
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



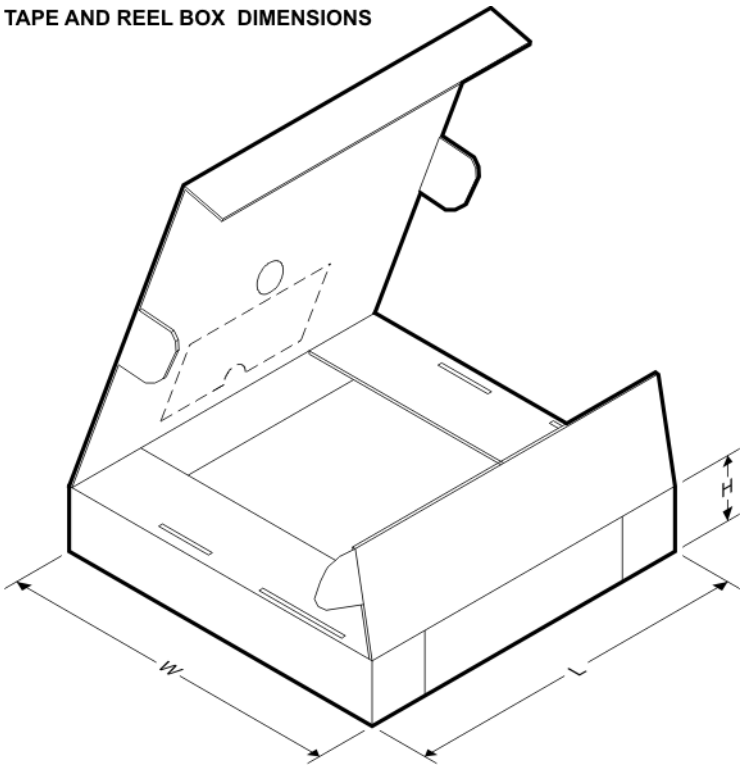
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1121IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1121IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1221IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF1221IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

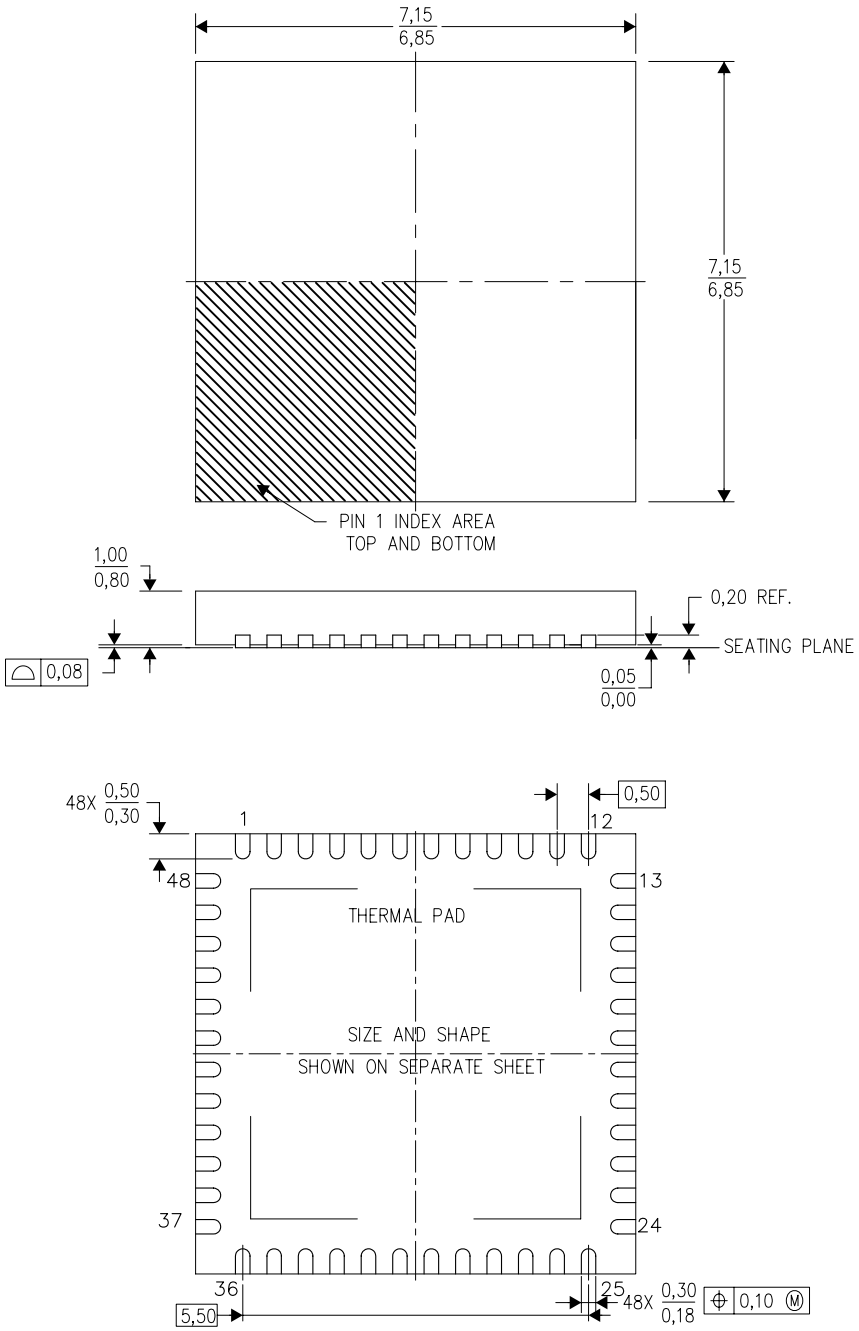
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1121IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
TRF1121IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
TRF1221IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
TRF1221IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

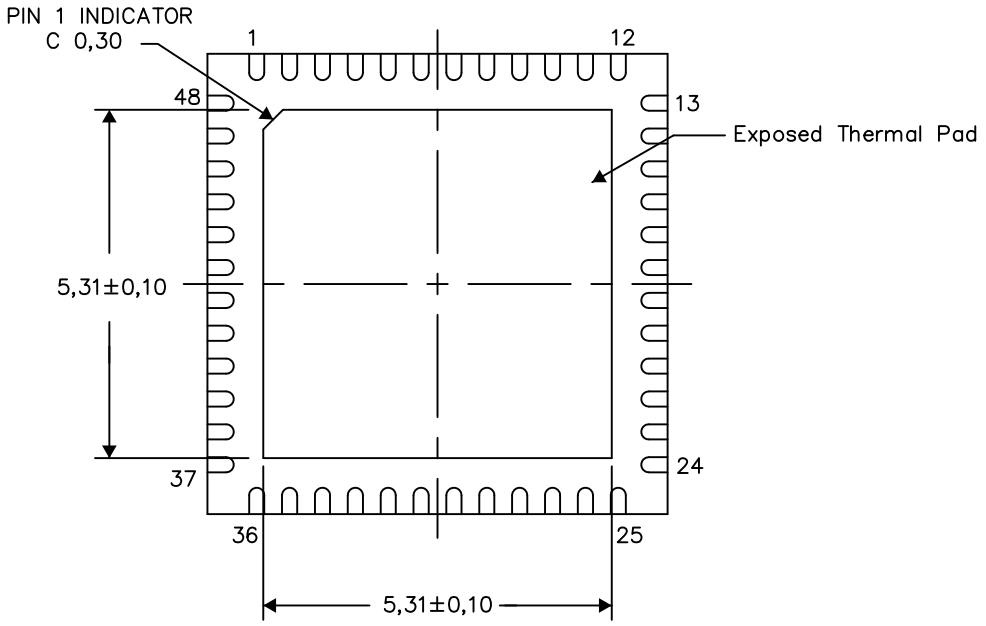
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206354–4/V 06/13

NOTE: All linear dimensions are in millimeters

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